Amendments to the Specification

Please replace paragraph [0025] with the following rewritten paragraph:

-- **[0025]** Figure 5 shows the final device following the deposition of top metal layer (7) and the etching of that layer into columns orthagonal to the rows. The result of this process will result in a 2 dimensional array of rectifying contacts (in this case, schottky diodes). The rows will be connected by the top ~~Metal 3~~ metal layer (7) and the columns will be connected by the bottom ~~Metal 1~~ metal layer (2). This top layer is expected to be about 2000 Å thick, but should be thick enough to carry enough current to provide the operational speed desired given any circuit capacitances without creating any of the previously mentioned aspect ratio problems when the columns are etched.--

Please replace paragraphs [0027] and [0028] with the following rewritten paragraphs:

--**[0027]** Figure 6 shows the result of this process if repeated on a substrate which has already had this process performed once. Note that the first layer will most likely be planarized with a polishing step before depositing an insulating film to start the second layer. In the case of the DRS memory constructed in multiple layers, these layers can be wired mostly in parallel (as described in U.S. Patent 5,889,694), only the bonding pads (9) would be interconnected by vias. As can be seen, the structure is identical except for the inclusion of vias (8) to interconnect the bonding points for power, ground and the complementary address inputs of each layer. The data bonding pads would be brought to the surface layer independently so that each data bonding pad would connect to a single layer. Other configurations of wiring are possible. For example, if the data lines of each layer were interconnected by vias and separation was instead accomplished by having

some address lines connected to specific layers so as to in effect enable only a single layer at a time and thereby multiplex the data connections. This would be the equivalent of implementing the selective powering of the device as is disclosed in U.S. Patent 5,889,694 whereby each individually powered section of the device was comprised in a separate layer.

[0028] Figure 7 shows an interconnection technique for the rows (and would be repeated for the columns) to enable the quick and inexpensive testing of the device. The most common faults expected to occur during the fabrication of the present invention are breaks in a line or shorts between two adjacent lines. With the present interconnection technique, all the alternate rows are connected end to end with a top layer connection thereby creating two conductive snakes — one comprising all the even numbered rows ~~(9)~~ (10) and the other comprising all the odd numbered rows ~~(10)~~(11). By doing so, one can test the device by probing the two ends of each snake and checking for continuity. This will enable instantaneously checking the all the rows for any breaks with just four probe points. Also, shorts between rows can be identified simultaneously by checking for any continuity between the two snakes. The columns would be simultaneously checked in an identical fashion. Also, in the same way and at the same time, the device can be checked for shorts between the top columns and bottom rows (taking care to select one range of voltage levels for the rows and another range of voltage levels for the columns such that the diodes are reverse biased). By combining this test technique with the multiple stacked rectifying towers design, if a device passes this instantaneous test, one can be highly confident of having a working device. After identifying any defective devices (which, if the devices are manufactured inexpensively enough, would most likely

just be marked to be discarded), these top layer connections are etched away to separate the lines or the edges of the chips where the interconnections are found could be cut back just enough to remove those edges and their interconnections.--

Please replace the abstract with the following rewritten abstract:

~~--The present invention is a means for constructing a~~A high density memory device ~~for very low cost by fabricating the device~~is fabricated three dimensionally in layers. To keep points of failure low, address decoding circuits are included within each layer so that, in addition to power and data lines, only the address signal lines need be interconnected between the layers~~— not the exponentially greater number of decoded rows and columns. Furthermore, to keep the testing of the device low in cost, a row and column interconnect means is disclosed for testing the any two-dimensional array within the three-dimensional array with a single continuity and short-circuit test.--~~